

FIG. 1

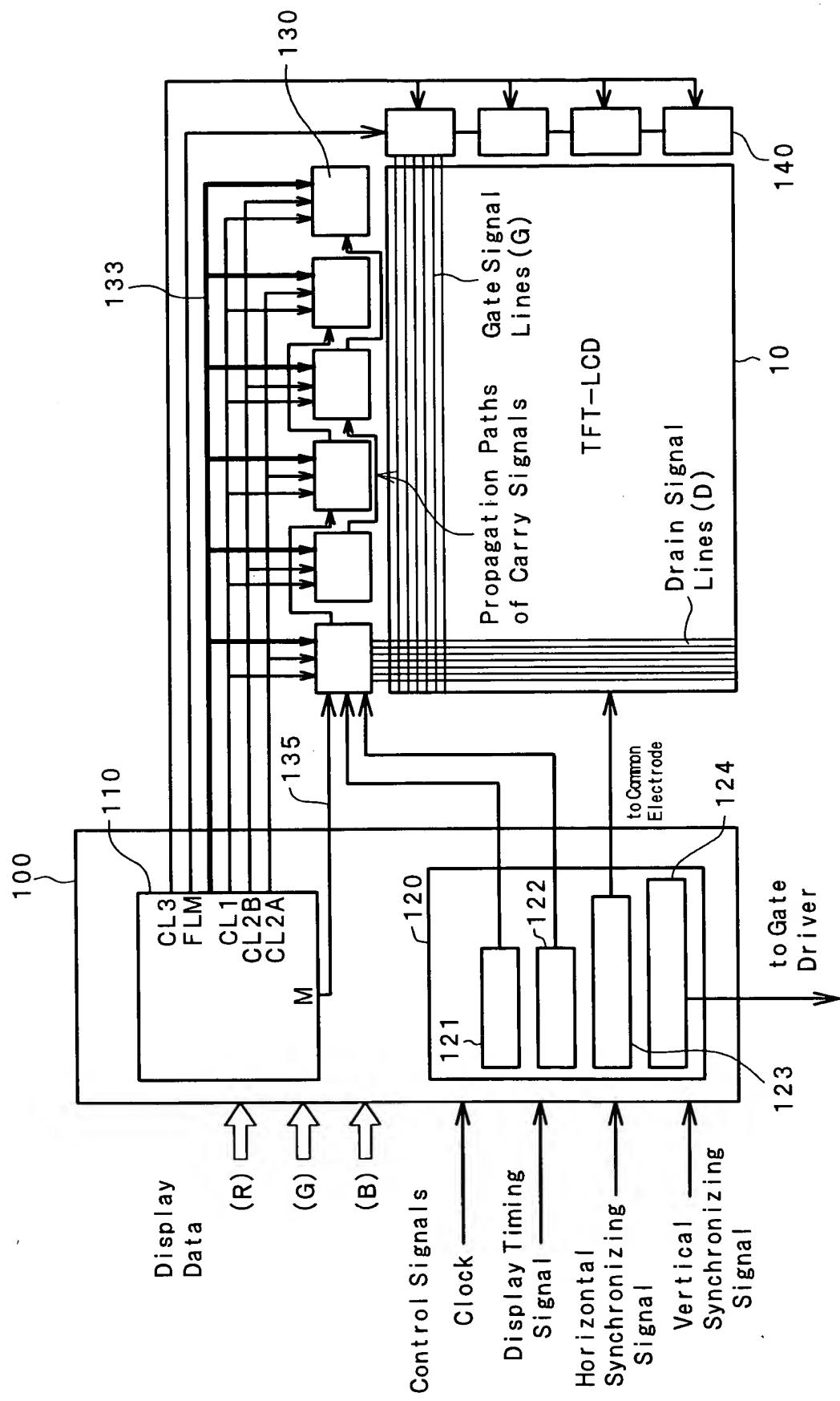


FIG. 2

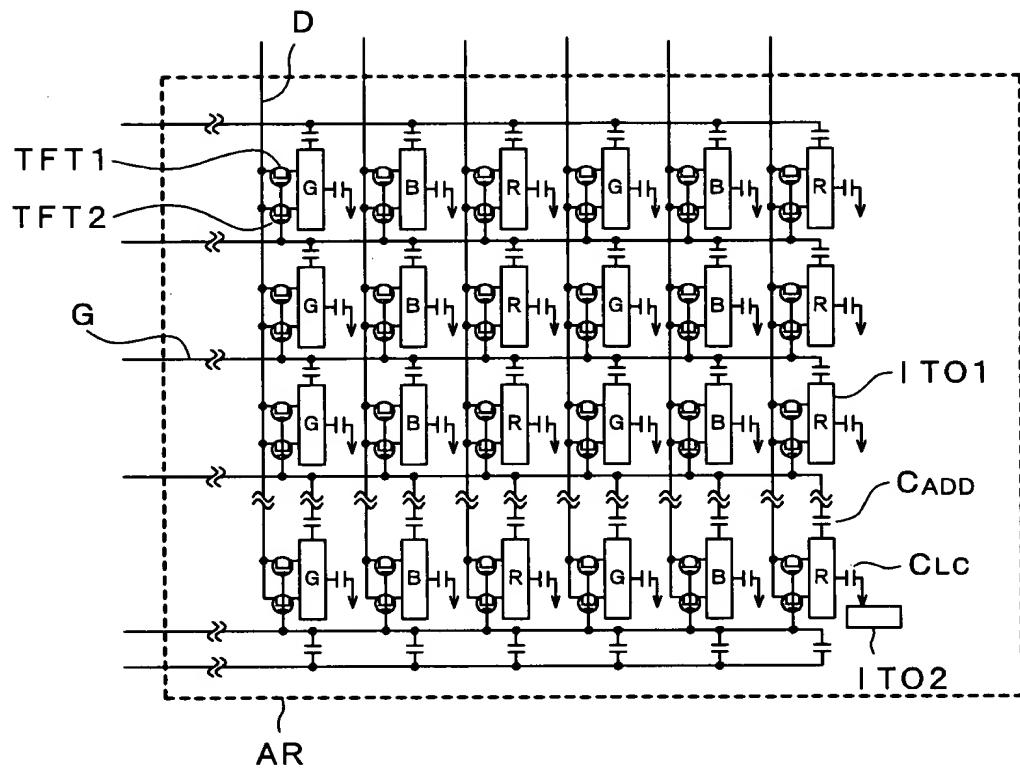


FIG. 3

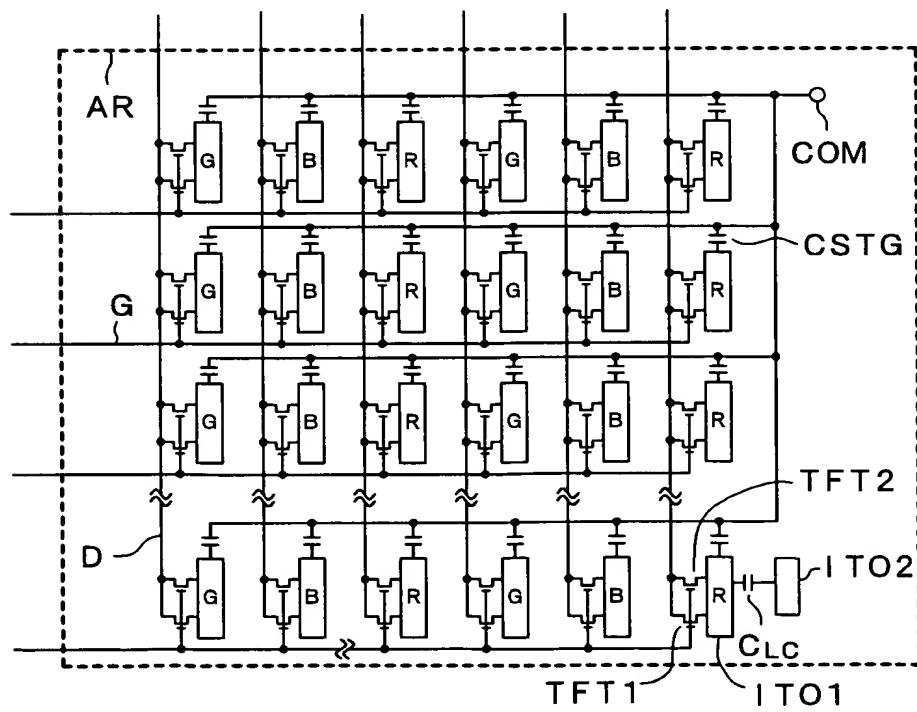


FIG. 4

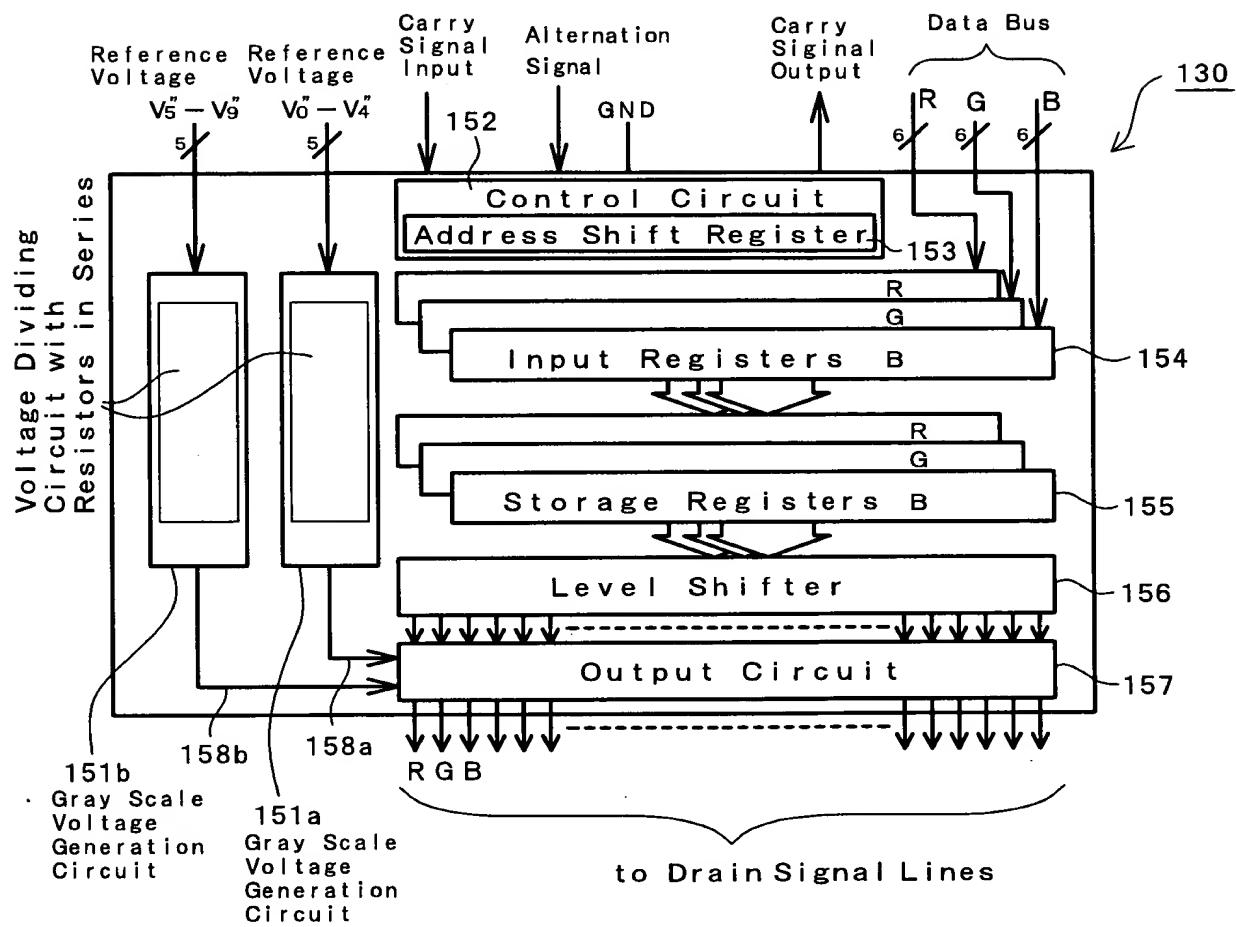


FIG. 5

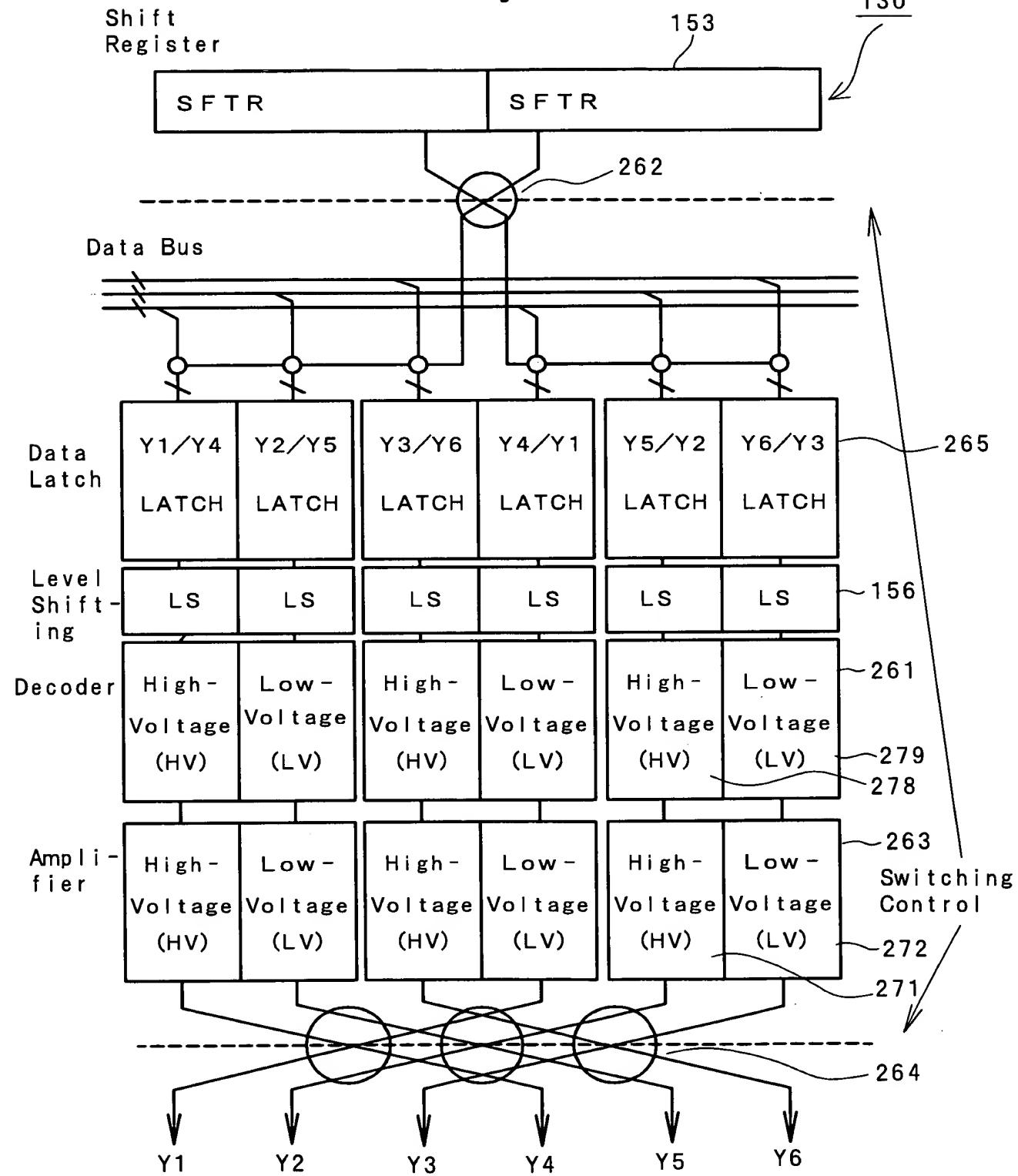


FIG. 6A

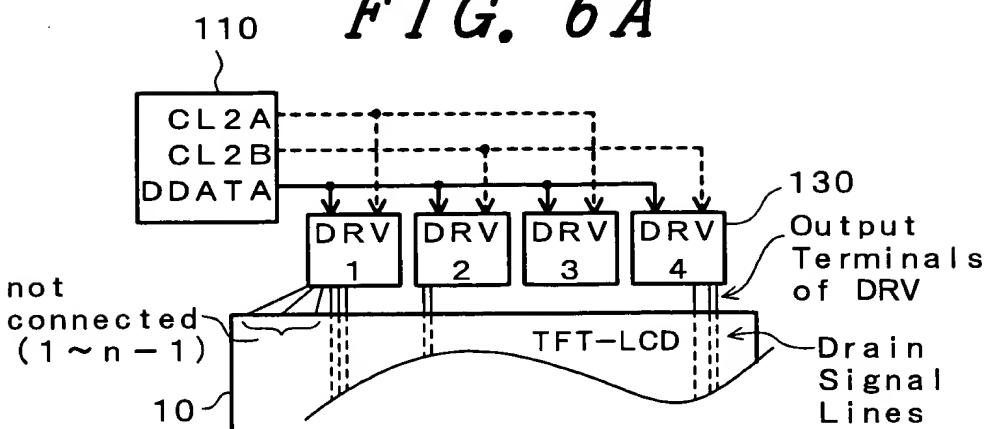


FIG. 6B



FIG. 6C

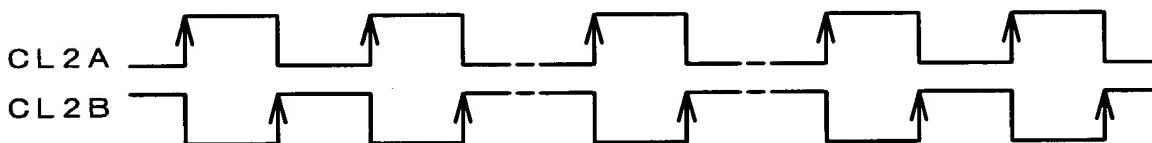


FIG. 7

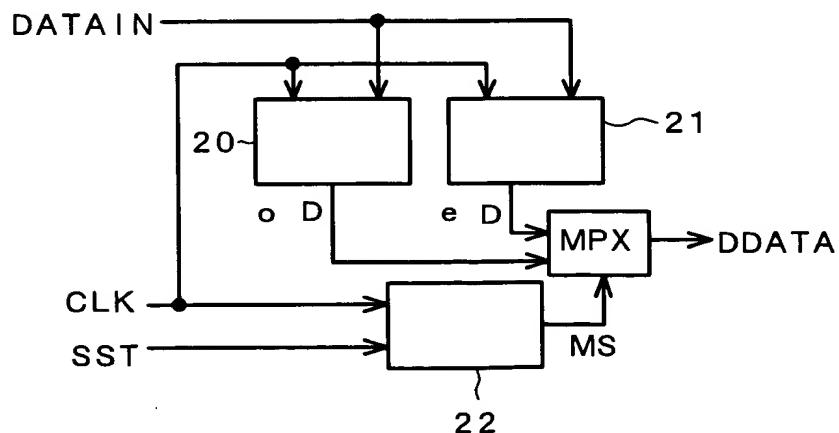


FIG. 8A

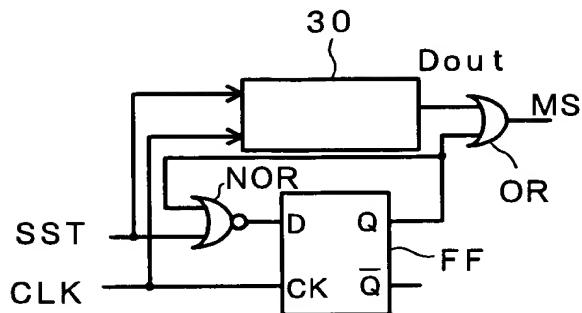


FIG. 8B

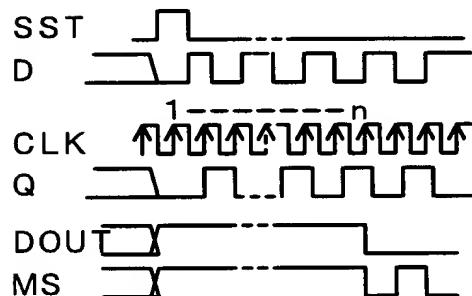


FIG. 9A

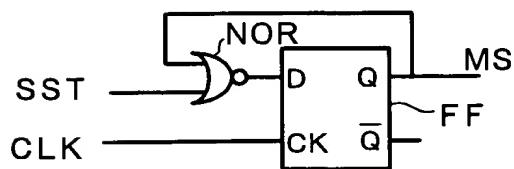


FIG. 9B

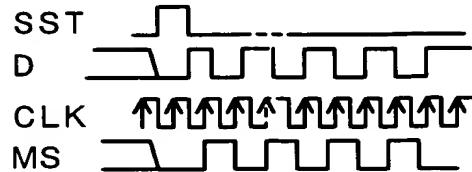


FIG. 10

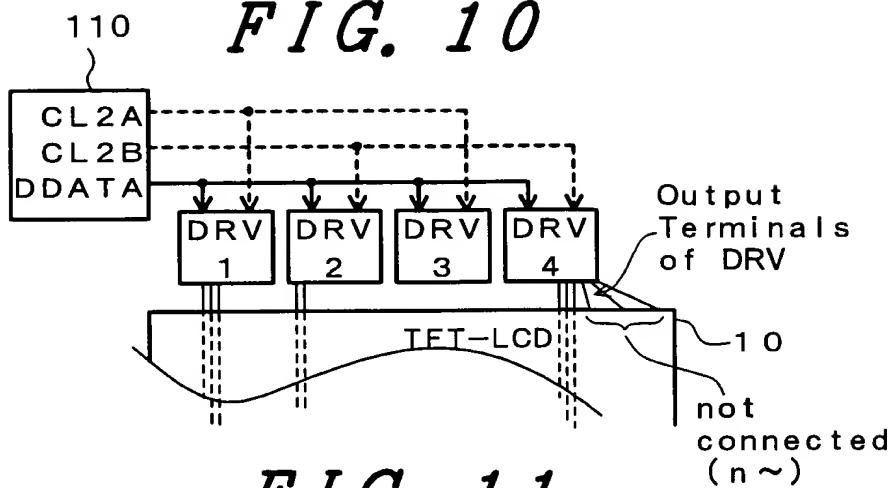


FIG. 11

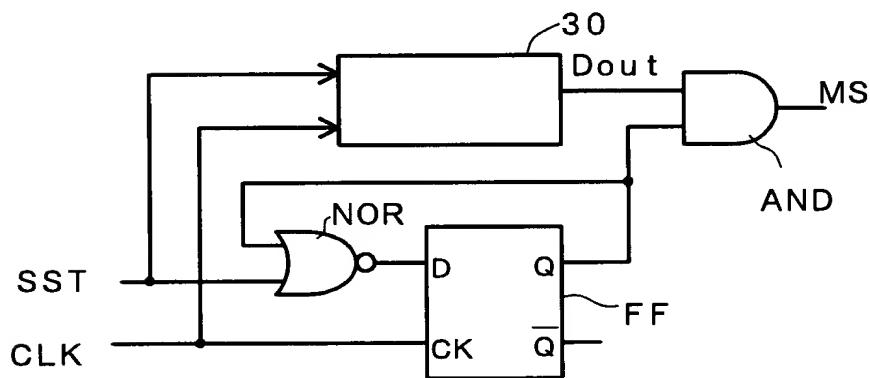


FIG. 12A

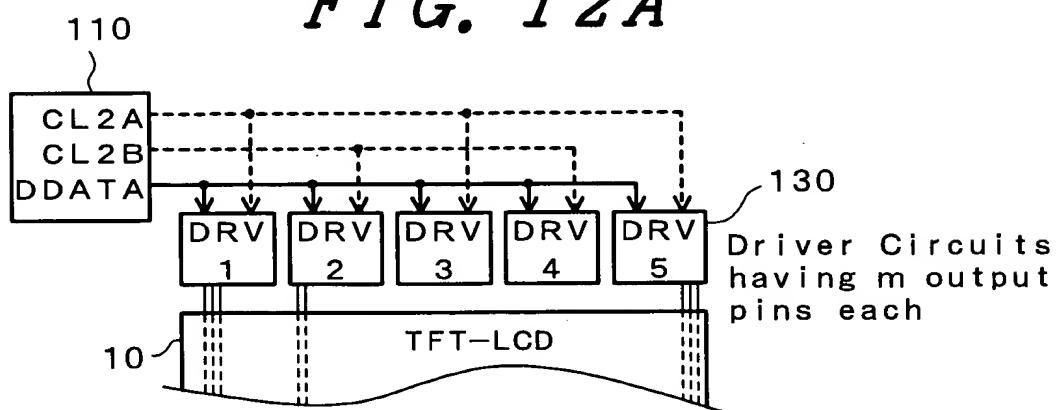


FIG. 12B

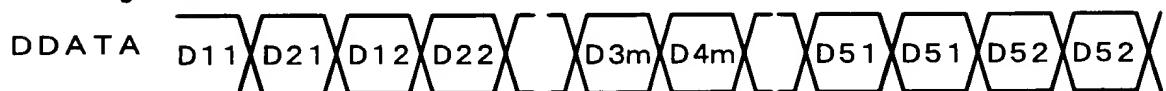


FIG. 12C

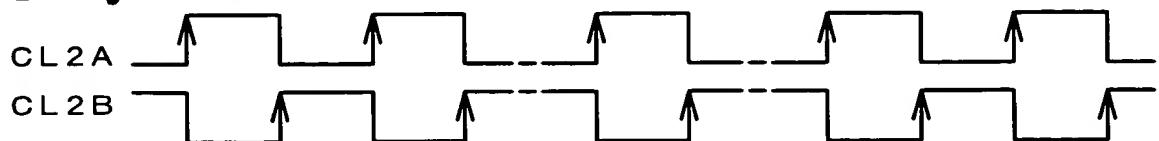


FIG. 13

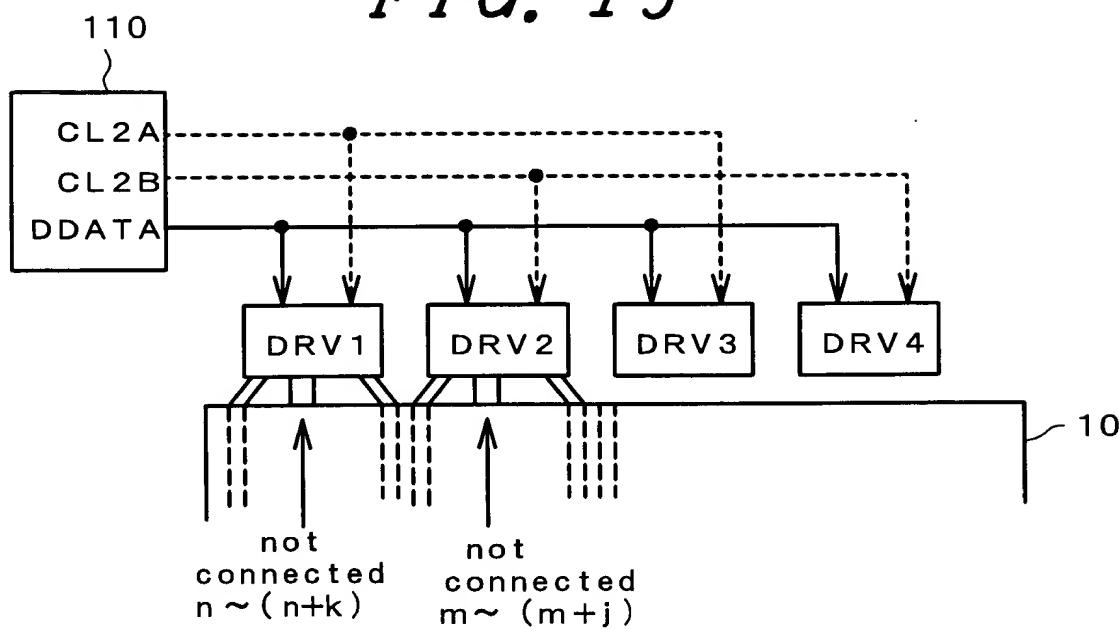


FIG. 14

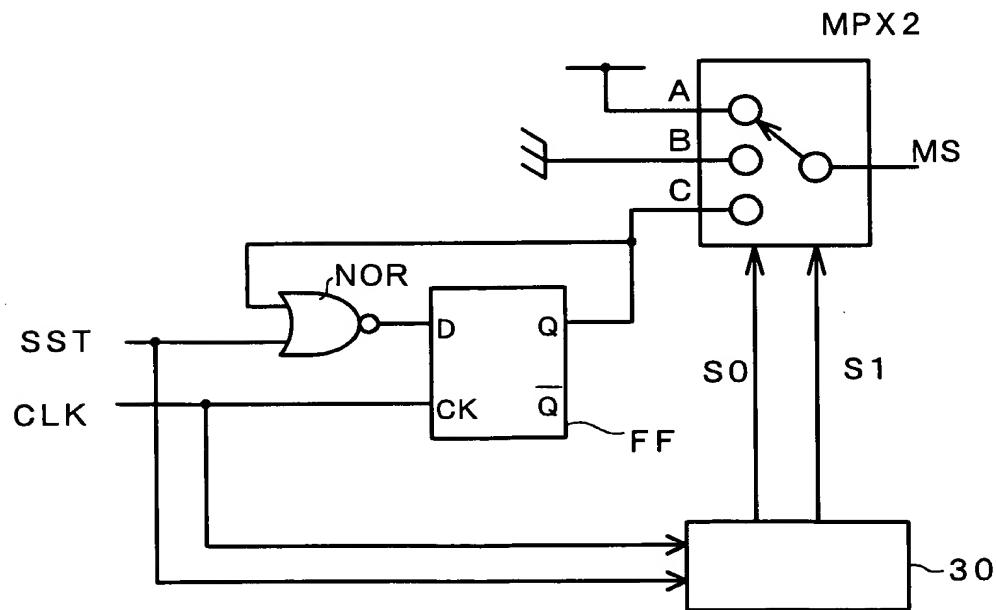
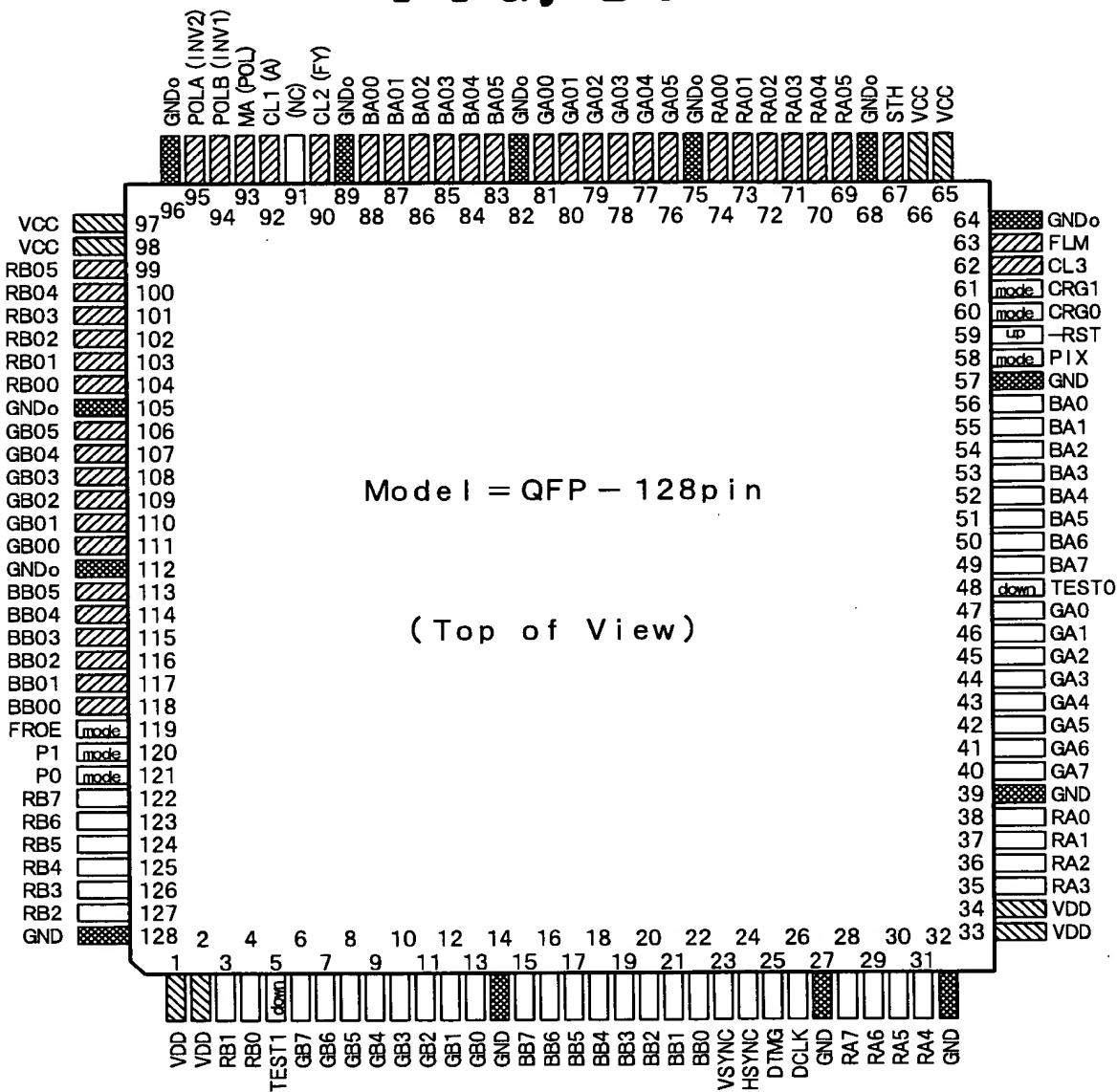


FIG. 15



RA[7:0], GA[7:0], BA[7:0] : For Input Data to First Pixels
RB[7:0], GB[7:0], BB[7:0] : For Input Data to Second Pixels

DCLK : Reference Clock (Input)

DTMG : Display Timing Signal (Input)

HSYNC : Horizontal Synchronizing Signal (Input)

VSYNC : Vertical Synchronizing Signal (Input)

PIX : High - Interface for Second Pixels Input (Mode Pin)
Low - Interface for First Pixels Input

 Power Source ; 3.3[V] (VDD)  GND (VSS)

 INPUT (CMOS Interface)  OUTPUT

 INPUT (Pull Up)  INPUT (Pull Down)

FIG. 16

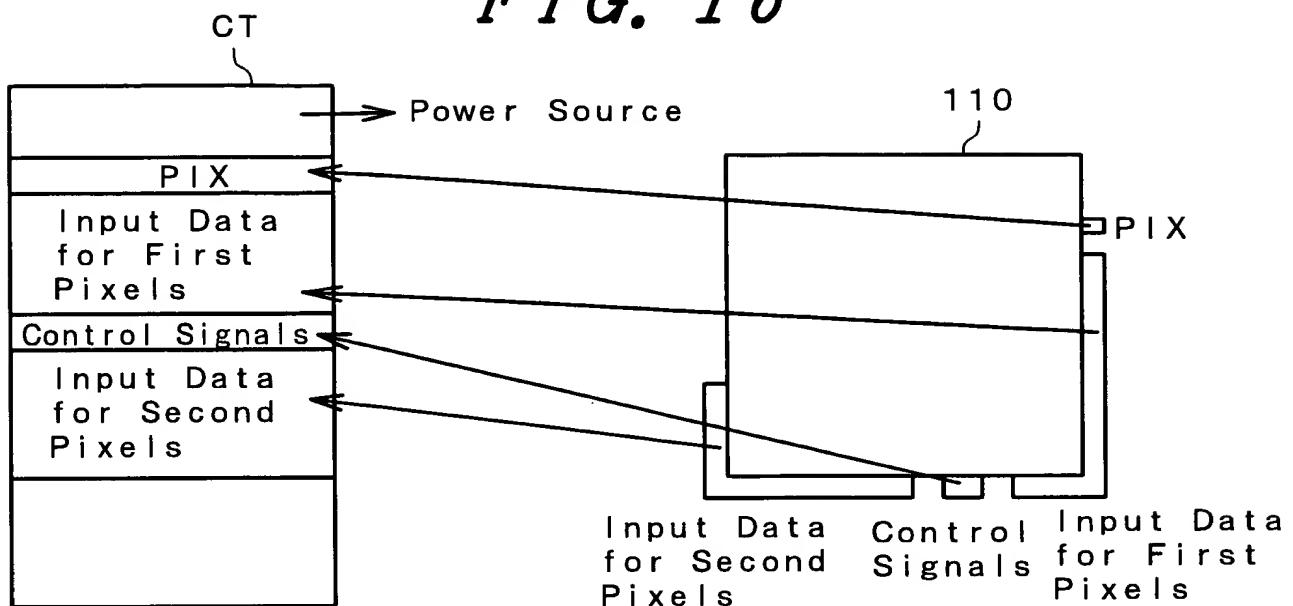


FIG. 17

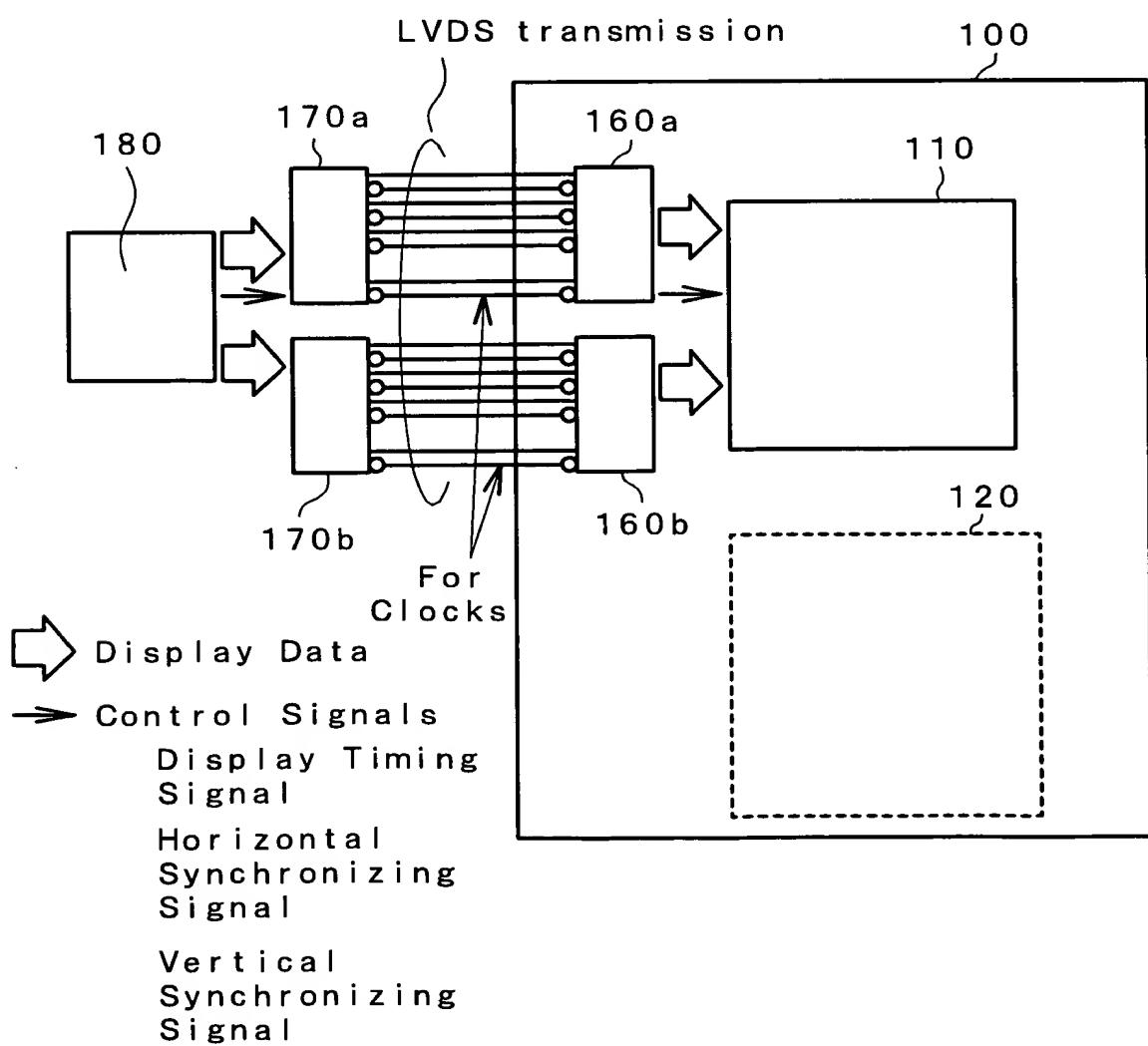


FIG. 18

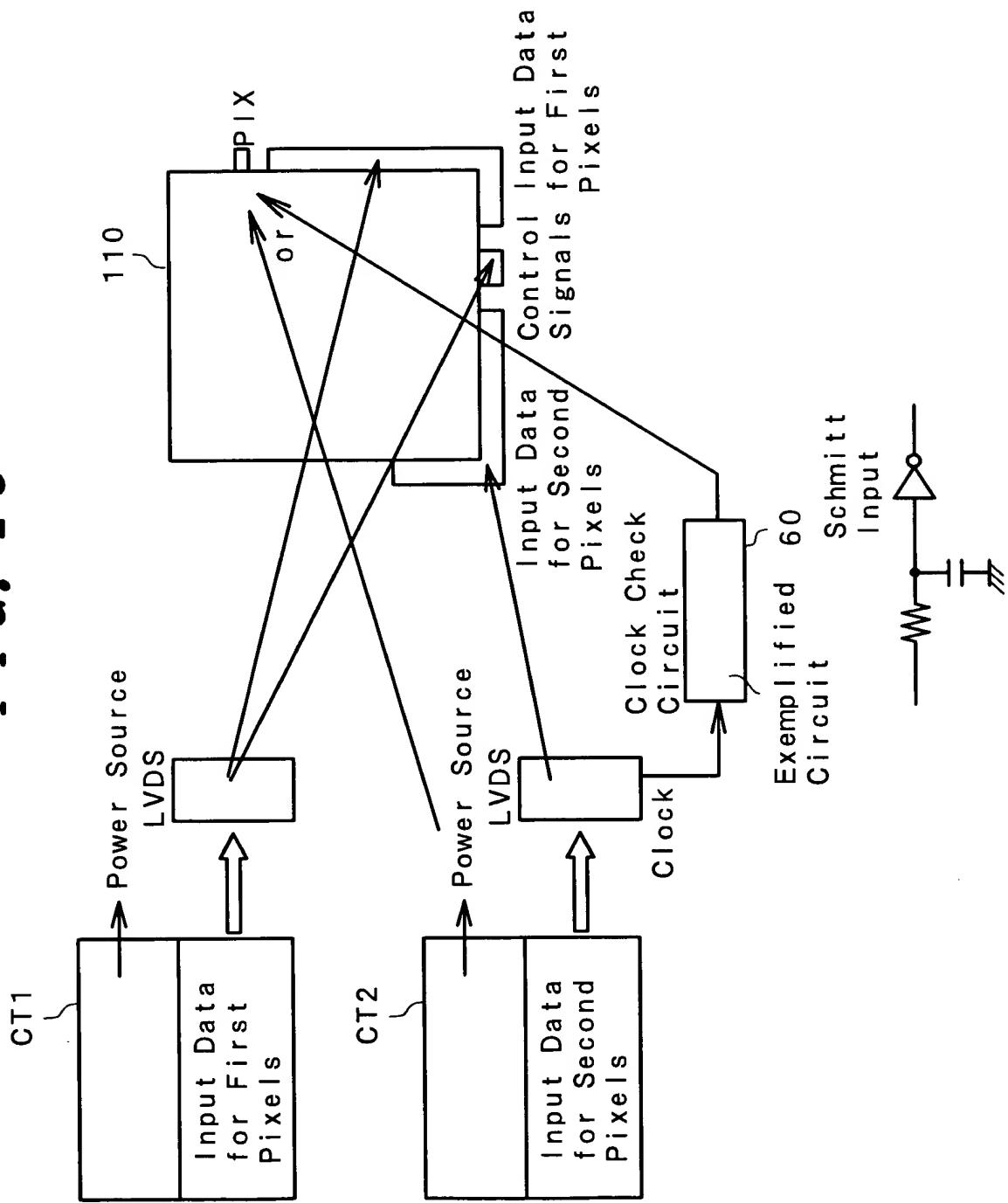


FIG. 19A

Interface for Single Pixel Line

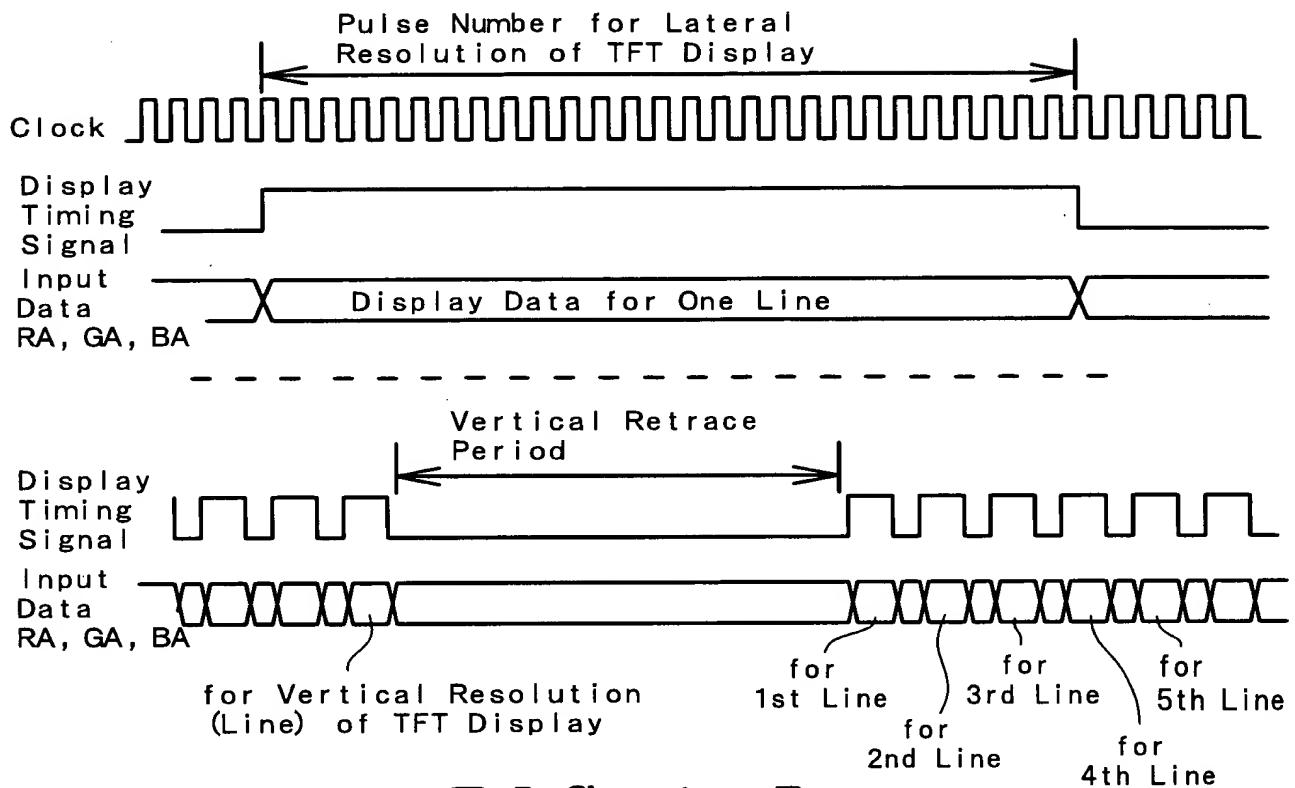
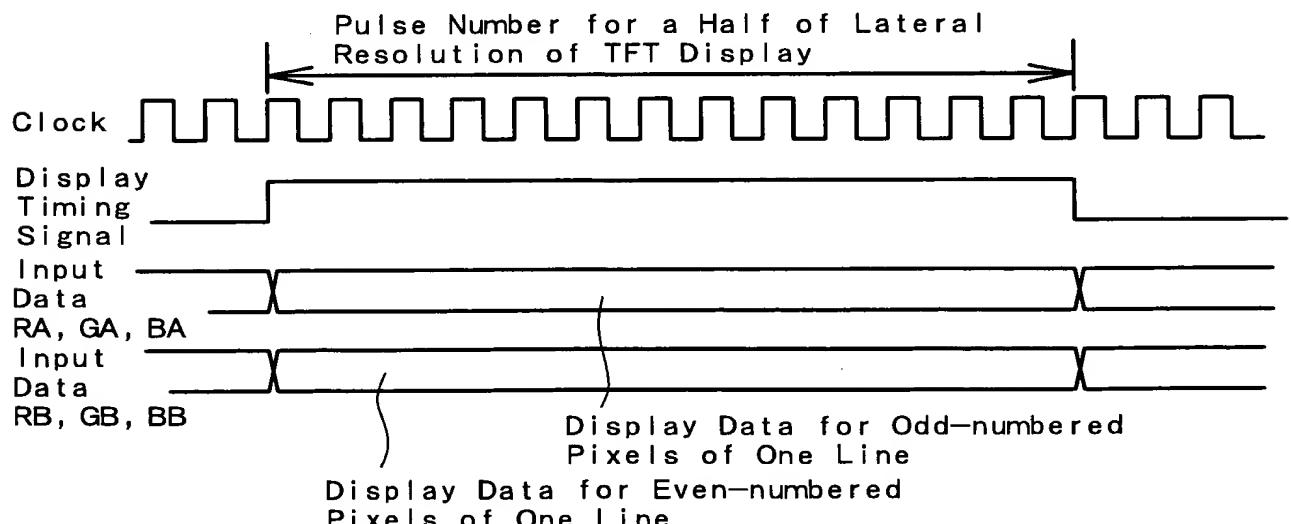


FIG. 19B

Interface for Dual Pixel Line



Clock period is Two-times Long as that
for Single Pixel Line

(Timing for Vertical Retrace Period is
same as that for Single Pixel Line)

FIG. 20

